THAT WHICH IS CLAIMED IS:

1. A power down circuit for use in a System on Chip SOC, comprising:

a plurality of circuit blocks (112, 114) in said SOC, each of said circuit blocks having a local clock (166);

a system clock (130) coupled to one or more of said plurality of circuit blocks (112, 114) and structured to act as said local clock (166) of selected ones of said plurality of circuit blocks;

a power control manager coupled to one of said plurality of circuit blocks (112, 114) and structured to provide a signal at least partially determining whether said system clock (130) will act as said local clock (166) of said one of the circuit blocks; characterized in that, in said one of the circuit blocks (112, 114) contains a local power control (150) structured to selectively maintain the system clock (130) acting as said local clock (166) said block after said local power control (150) receives a signal to shutdown (142) said block from said power control manager (140), if said block is busy when said signal to shutdown said block is received.

2. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said local power control (150) is a clock separation circuit coupled to the power control manager (140) and structured to prevent said system clock (130) from acting as said local clock (166) in said block that is receiving said shutdown signal (142) while in an idle state.

3. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said power control module (140) is coupled to said local power control (150) through a clock enable line (142).

4. A power down circuit for use in the System on Chip SOC according to Claim 3, further characterized in that said local power control (150) includes a logic circuit (156, 158) coupled to said clock enable line (142), a busy line (154), and said system clock (130), and said logic circuit is structured to generate said local clock (166) at an output of said logic circuit (156, 158) responsive to signals on said clock enable line (142), said busy line (154), and said system clock (130).

5. A power down circuit for use in the System on Chip SOC according to Claim 1, further characterized in that said power control module (140) comprises a register (146) coupled to a clock enable line (142) of each of said circuit blocks (112, 114), and in that said register (146) stores a datum indicating a state of one or more of the clock enable lines (142) respectively coupled to it.

6. A power down circuit for use in the System on Chip SOC according to Claim 5, characterized in that it further comprises a CPU coupled to said power control module (140), the CPU able to determine said states of said circuit blocks (112, 114 by querying said register (146).

7. A power down circuit for use in the System on Chip SOC according to Claim 1, characterized in that more than one system clocks are present in said System on Chip and are respectively structured to act as said local clock (166) of selected ones of said plurality of circuit blocks.

8. A method of powering down individual circuit blocks of a plurality of circuit blocks within a System on Chip, comprising the steps of:

generating a system clock signal (130) that is coupled to said plurality of circuit blocks (112, 114) and can be used as a local clock (166) for said plurality of circuit blocks;

generating a signal to power down (142) selected of the plurality of circuit blocks;

transmitting said signal to power down (142) said selected circuit blocks to a local power control (150); characterized in that the method further comprises:

accepting said signal to power down (142) at said local power control (150) in each of said selected circuit blocks (112, 114);

accepting a current state of said respective circuit block on a busy line (154); and

shutting down said selected circuit blocks after comparing both said signal to power down and said current state of said respective circuit block.

9. A method of powering down individual circuit blocks according to Claim 8, characterized in that said method further comprises preventing said shutdown of said selected circuit blocks if either said

signal to power down is not received, or if said selected circuit blocks are currently busy.

10. A method of powering down individual circuit blocks according to Claim 9, characterized in that shutting down said selected circuit blocks comprises preventing said system clock (130) from acting as said local clock (166) in said selected circuit blocks.

11. A method of powering down individual circuit blocks according to Claim 10 characterized in that preventing said system clock (130) from acting as said local clock (166) comprises disconnecting said system clock (130) from said local clock (310) only when those circuit blocks that have received said signal to power down (142) selected circuit blocks are idle.